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10-06-05

PATENT APPLICATION

ATTORNEY DOCKET NO. 10970696-3

AF/IFW

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Tony M. Brewer

Confirmation No.: 7372

Application No.: 10/650,105

Examiner: B. Peikari

Filing Date: 08-25-2003

Group Art Unit: 2189

Title: VIRTUAL MEMORY TRANSLATION CONTROL BY TLB PURGE MONITORING

Mail Stop Appeal Brief-Patents
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TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **08-05-2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Typed Name: Joy H. Perigo

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Respectfully submitted,

Tony M. Brewer

By _____

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Docket No.: 10970696-3
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Tony M. Brewer

Application No.: 10/650,105 | Confirmation No.: 7372

Filed: August 25, 2003 | Art Unit: 2189

For: VIRTUAL MEMORY TRANSLATION CONTROL BY TLB PURGE MONITORING | Examiner: B. Peikari

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on August 5, 2005, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

X. Related Proceedings
Appendix A Claims

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 17 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 0

2. Claims withdrawn from consideration but not canceled: 0

3. Claims pending: 17

4. Claims allowed: 0

5. Claims rejected: 1-17

C. Claims On Appeal

The claims on appeal are claims 1, 4, and 12.

Claims 1-17 are rejected under the judicially-created doctrine of double patenting over claims 1-10 of *Brewer* (U.S. Patent No. 6,668,314, hereinafter *Brewer '314*). Claims 6-

11 and 15-17 are rejected under the judicially-created doctrine of double patenting over claims 12-16 of *Brewer* (U.S. Patent No. 5,966,733, hereinafter *Brewer* '733). Appellant has proposed filing a terminal disclaimer in compliance with 37 C.F.R. § 1.321(b) if the Examiner's rejection still properly stands after an indication of allowability over prior art of record in the present case.

IV. STATUS OF AMENDMENTS

Appellant filed an Amendment After Final Rejection on July 5, 2005. The Examiner responded to the Amendment After Final Rejection in an Advisory Action mailed July 26, 2005. In the Advisory Action, the Examiner indicated that Appellant's proposed amendments to claims 1, 5, and 6 are entered.

Accordingly, the claims enclosed herein as Appendix A incorporate the amendments to claims 1, 5, and 6, as indicated in the paper filed. The claims in Appendix A also incorporate the amendments made in the paper filed by Appellant on May 5, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

According to claim 1, a method for controlling virtual memory address translation during data movement operations enabled in a hardware environment (page 44, lines 15-24; Figure 15), comprising the steps of:

monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory (page 45, line 19-page 46, line 9; 1502 of Figure 15); and

upon detection of a TLB purge prior to completion of the data movement operation, aborting the data movement operation pending reestablishment of accurate virtual-memory-to-physical-memory mapping (page 46, lines 10-19; 1510-1513 of Figure 15).

According to claim 2, the method of claim 1, further comprising the step of enqueuing status information on whether the data movement operation completed or was aborted (page 46, lines 13-17).

According to claim 3, the method of claim 2, in which said status information includes identification of data that was successfully moved prior to an abort (page 46, lines 20-24).

According to claim 4, the method of claim 1, in which the data movement operation is a data copying operation (page 44, lines 10-14).

According to claim 5, a method for controlling virtual memory address translation during data movement operations enabled in a hardware environment, comprising the steps of:

monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory (page 45, line 19-page 46, line 9);

upon detection of a TLB purge prior to completion of the data movement operation, aborting the data movement operation pending reestablishment of accurate virtual-memory-to-physical-memory mapping (page 46, lines 10-19); and

enqueuing status information on whether the data movement operation completed or was aborted (page 46, lines 13-17).

According to claim 6, hardware for controlling virtual memory address translation during data operations involving physical movement of data, the hardware comprising:

means for setting a first flag upon initiation of a data operation (page 45, lines 9-13);

means for periodically monitoring for translation lookaside buffer (TLB) purges (page 45, lines 19-20);

means for translating virtual address space to physical address space (page 45, lines 20-23);

means for setting up one or more input registers on a data mover (page 45, lines 23-25);

means, responsive to said means for translating and said means for setting up, for clearing the first flag if a TLB purge has been detected (page 46, lines 3-5); and

means for aborting the data operation and then enqueuing a first operation completion status if a TLB purge is detected before physical movement of data is complete (page 46, lines 13-17).

According to claim 7, the hardware of claim 17, in which the second operation completion status indicates completion of the data operation (page 46, lines 20-24).

According to claim 8, the hardware of claim 6, in which the first operation completion status identifies data that was successfully moved prior to the abort (page 46, lines 12-16).

According to claim 9, the hardware of claim 6, in which the data operation is a data copying operation (page 44, lines 10-14).

According to claim 10, the hardware of claim 16, in which the means for clearing the first flag and setting a second flag is enabled if a TLB purge has not been detected before physical data movement is to commence (page 45, line 29-page 46, line 5).

According to claim 11, the hardware of claim 6, in which the means for clearing the first flag is enabled if a TLB purge has been detected before physical data (page 46, lines 3-5).

According to claim 12, the method of claim 1, wherein said occurrence of a TLB purge is indicative that a change in virtual-memory-to-physical-memory mapping has occurred (page 45, lines 7-9).

According to claim 13, the method of claim 5, wherein said occurrence of a TLB purge is indicative that a change in virtual-memory-to-physical-memory mapping has occurred (page 45, lines 7-9).

According to claim 14, the method of claim 5 further comprising:

enqueuing status information including identification of data that was successfully moved prior to the abort (page 46, lines 12-16).

According to claim 15, the hardware of claim 6, wherein an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory is indicative that a change in virtual-memory-to-physical-memory mapping has occurred (page 45, lines 7-9).

According to claim 16, the hardware of claim 6 further comprising:

means, responsive to said means for translating and said means for setting up, for

clearing the first flag and setting a second flag if a TLB purge has not been detected (page 45, line 29-page 46, line 5);

means for examining the second flag (page 46, lines 5-6); and

means for commencing physical movement of data if the second flag is set (page 46, lines 8-9).

According to claim 17, the hardware of claim 6 further comprising:

means for enqueuing a second operation completion status if a TLB purge is not detected before physical movement of data is complete (page 46, lines 20-24).

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

A. First Ground of Rejection

Claims 1, 4, and 12 are rejected under 35 U.S.C. § 102(e) as being anticipated by *Wu et al.* (U.S. Patent No. 5,906,001, hereinafter *Wu*).

VII. ARGUMENT

A First Ground of Rejection

Claims 1, 4, and 12 are rejected under 35 U.S.C. § 102(e) as being anticipated by *Wu*.

"It is well settled that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ.2d 1051, 1053 (Fed. Cir. 1987). Appellant respectfully asserts that *Wu* does not teach each and every element of each of claims 1, 4, and 12, and accordingly does not meet the *Verdegaal* requirements.

Claim 1 recites "monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory." The Examiner states that *Wu* teaches the recited limitation at col. 2, lines 33-54. Appellant respectfully disagrees. The cited portion of *Wu* teaches methods of maintaining coherency among several caches. *Wu* teaches "snooping" for maintaining coherency in data caches. *See* col. 2, lines 42-44. However, *Wu* also teaches

that "while snooping is commonly used to maintain coherency in data caches, it is typically not employed for maintaining TLB coherency." *Id.* *Wu* further teaches a TLB "shootdown" operation. *See* col. 2, line 45-col. 3, line 11. However, the shootdown operation of *Wu* appears to be a software-based operation. For example, the shootdown operation executes an INVPLG instruction that is used by an operating system or software routine. *See* col. 2, lines 19-29. The shootdown operation may also use a software interrupt instruction, INT. *See* col. 2, lines 64-11. However, these methods do not teach monitoring, as a hardware operation, for an occurrence of a TLB purge during setup and execution of a data movement operation from virtual memory. Accordingly, *Wu* does not teach "monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory" as required in claim 1. Thus, *Wu* does not anticipate claim 1.

Claims 4 and 12 depend directly from claim 1. Because claims 4 and 12 depend directly from claim 1, they contain all limitations of the base claim. As shown above, *Wu* does not teach all limitations of claim 1. Accordingly, *Wu* does not teach all limitations of claims 4 and 12. Thus, *Wu* does not anticipate claims 4 and 12. Appellant respectfully requests that the rejection of record be withdrawn and claims 1, 4, and 12 passed to allowance.

In the Advisory Action mailed July 26, 2005, the Examiner states that claim 1 is "nowhere limited to strictly hardware operation." Appellant respectfully disagrees. Claim 1, as shown above, recites "monitoring, as a hardware operation...." Appellant asserts that the recited limitation clearly limits monitoring as a hardware operation.

The Examiner further states in the Advisory Action that "it is clear from the specification that such 'monitoring' involves both hardware and software." Appellant assumes that this statement refers to arguments made by the Examiner in the Office Action mailed May 5, 2005. On page 8 of the May 5, 2005 Office Action, the Examiner states that "applicant's operations are not *entirely* or *exclusively* hardware based..." and provides citations to page 1, 11, and 18 of the specification in support. Regarding the citation on page 1 of the specification, which recites "[t]he invention is operable in an environment in which

data movement is performed largely by hardware rather than software...," Appellant respectfully asserts that one of ordinary skill in the art would understand that certain embodiments of the invention operate in environments in which data movement is performed largely by hardware and/or environments in which data movement is provided entirely by hardware, especially when considered in view of the numerous examples of embodiments of the present invention "enabled in hardware rather than software". *See* page 13, lines 7-14. *See also* page 10, lines 1-5 (performing operations integral to data movement with hardware rather than software); page 52, lines 1-5 (optimizing aspects of data movement operations by performing functions on hardware rather than software).

Regarding the citation on page 11, Appellant respectfully asserts that the Examiner has paraphrased this part of the specification. Appellant respectfully points out that the paraphrased text, when taken in context, refers to an embodiment illustrated in Figure 1 of the application, not all embodiments. In the same paragraph from which the Examiner's paraphrased citation was taken, the specification recites that "...these phases or aspects are enabled by hardware under the invention." *See* page 11, lines 8-14.

In the May 5, 2005 Office Action, the Examiner again paraphrases material on page 18 of the specification that is directed to a particular embodiment of the present invention. *See* Final Office Action, page 8. Again, taken in its entirety, Appellant respectfully asserts that the application clearly supports the claim element recited by claims 1, 4, and 12 of "monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory."

The Examiner further states in the Advisory Action that pages 18 and 38-39 of the specification teach TLB monitoring and messaging with "reliance on software." Regarding page 18, Appellant has already asserted that taken in its entirety, the application clearly supports "monitoring, as a hardware operation...." Regarding pages 38-39 of the application, TLB monitoring is not mentioned by this citation, and thus does not support the Examiner's argument that "monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge" as recited by claim 1 is taught by the specification as

comprising software operations. Appellant has disclosed several embodiments of the present invention in the specification, some of which are broader in scope than the appealed claims, but which do not limit the claims to those embodiments.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Appellant on May 5, 2005 and July 5, 2005.

IX. EVIDENCE

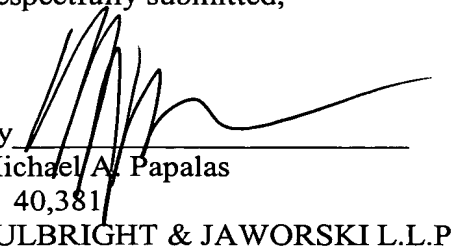
No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: October 5, 2005

Respectfully submitted,



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Dated: October 5, 2005

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Joy H. Perigo

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/650,105

1. (Previously Presented) A method for controlling virtual memory address translation during data movement operations enabled in a hardware environment, comprising the steps of:

monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory; and

upon detection of a TLB purge prior to completion of the data movement operation, aborting the data movement operation pending reestablishment of accurate virtual-memory-to-physical-memory mapping.

2. (Original) The method of claim 1, further comprising the step of enqueuing status information on whether the data movement operation completed or was aborted.

3. (Original) The method of claim 2, in which said status information includes identification of data that was successfully moved prior to an abort.

4. (Original) The method of claim 1, in which the data movement operation is a data copying operation.

5. (Previously Presented) A method for controlling virtual memory address translation during data movement operations enabled in a hardware environment, comprising the steps of:

monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory;

upon detection of a TLB purge prior to completion of the data movement operation, aborting the data movement operation pending reestablishment of accurate virtual-memory-to-physical-memory mapping; and

enqueuing status information on whether the data movement operation completed or was aborted.

6. (Previously Presented) Hardware for controlling virtual memory address translation during data operations involving physical movement of data, the hardware comprising:

means for setting a first flag upon initiation of a data operation;

means for periodically monitoring for translation lookaside buffer (TLB) purges;

means for translating virtual address space to physical address space;

means for setting up one or more input registers on a data mover;

means, responsive to said means for translating and said means for setting up, for clearing the first flag if a TLB purge has been detected; and

means for aborting the data operation and then enqueuing a first operation completion status if a TLB purge is detected before physical movement of data is complete.

7. (Previously Presented) The hardware of claim 17, in which the second operation completion status indicates completion of the data operation.

8. (Previously Presented) The hardware of claim 6, in which the first operation completion status identifies data that was successfully moved prior to the abort.

9. (Previously Presented) The hardware of claim 6, in which the data operation is a data copying operation.

10. (Previously Presented) The hardware of claim 16, in which the means for clearing the first flag and setting a second flag is enabled if a TLB purge has not been detected before physical data movement is to commence.

11. (Previously Presented) The hardware of claim 6, in which the means for clearing the first flag is enabled if a TLB purge has been detected before physical data.

12. (Previously Presented) The method of claim 1, wherein said occurrence of a TLB purge is indicative that a change in virtual-memory-to-physical-memory mapping has occurred.

13. (Previously Presented) The method of claim 5, wherein said occurrence of a TLB purge is indicative that a change in virtual-memory-to-physical-memory mapping has occurred.

14. (Previously Presented) The method of claim 5 further comprising:

enqueuing status information including identification of data that was successfully moved prior to the abort.

15. (Previously Presented) The hardware of claim 6, wherein an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory is indicative that a change in virtual-memory-to-physical-memory mapping has occurred.

16. (Previously Presented) The hardware of claim 6 further comprising:

means, responsive to said means for translating and said means for setting up, for clearing the first flag and setting a second flag if a TLB purge has not been detected;

means for examining the second flag; and

means for commencing physical movement of data if the second flag is set;

17. (Previously Presented) The hardware of claim 6 further comprising:

means for enqueuing a second operation completion status if a TLB purge is not detected before physical movement of data is complete.

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